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EXAMINER
SWICKHAMER, CHRISTOPHER M

ART UNIT	PAPER NUMBER
2697	19

DATE MAILED: 09/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/452,751	FIELD ET AL.	
	Examiner	Art Unit	
	Christopher M Swickhamer	2697	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to the Amendment filed 06/26/03. Claims 1-33 are pending. Currently no claims are in condition for allowance.

Information Disclosure Statement

2. The Examiner acknowledges receipt of the references listed in PTO form 1449, lines G-T of the IDS filed 08/30/02 (Paper No. 5).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 2, 5-18, 21-23, and 33 are rejected under 35 U.S.C. 102(b) as being anticipated by Van As et al (USP 5,327,428, hereinafter Van As). Referring to claim 1, Van As discloses a synchronous switch for a telecommunications node, comprising: a Pipeline Header Decoder (switch interface) operable to terminate a bus and to receive from the bus a frame having a plurality of time slots that are each operable to transport a traffic cell (Fig. 3-6 and 27-29, col. 8, lns. 13-25, col. 21, lns. 60-col. 22, lns. 15); a RX-FSM (switch controller) operable to determine a type for each traffic cell received at the Pipeline Header Decoder (switch interface) and to determine based on the slot type in the header for a traffic cell a queue (an address) for storing

the traffic cell in one of a plurality of queues (switch memory, col. 22, lns. 15-55); and the plurality of queues (switch memory) operable to receive the traffic cell from the Pipeline Header Decoder (switch interface) and the RX-FSM instructs the ADU modifier to split the multi-slot frame and send the basic slot to the appropriate queue (address) for storing the traffic cell from the RX-FSM (switch controller) and to store the traffic cell at the queue (address, col. 22, lns. 15-40).

- Referring to claim 2, Van As discloses the synchronous switch of Claim 1, further comprising: the Pipeline Header Decoder (switch interface) operable to extract a header for the traffic cell from a time slot transporting the traffic cell and to provide the header to the RX-FSM (switch controller); and the RX-FSM (switch controller) further operable to determine the type for the traffic cell based on the slot type information in the header (col. 21, lns. 60-col. 22, lns. 40).

- Referring to claim 5, Van As discloses the synchronous switch of Claim 1, wherein the Pipeline Header Decoder (switch interface), RX-FSM (switch controller), and a plurality of queues (switch memory) each operate at a framing period (synchronized frame pulse, Fig. 3-6, col. 12, lns. 1-30, col. 19, lns. 40-47, col. 24, lns. 60-65).

- Referring to claim 6, Van As discloses the synchronous switch of Claim 5, wherein the synchronized frame pulse is a 125 microsecond frame pulse (col. 12, lns. 1-30, col. 19, lns. 40-47, Fig. 3-6).

- Referring to claim 7, Van As discloses the synchronous switch of Claim 1, further comprising the Pipeline Header Decoder (switch interface) operable to terminate a plurality of point-to-point links of the bus and to receive from each link a frame having a plurality of the

time slots (Fig. 3-6, col. 8, lns. 13-25). A bus is an electrical connection that allows two or more connections to be connected together. This implies that the Pipeline Header decoder can receive the frames from multiple point-to-point links over the bus.

- Referring to claim 8, Van As discloses the synchronous switch of Claim 7, wherein the point-to-point links of the bus operate at disparate rates (col. 8, lns. 12-25). The data flowing over the point-to-point links have a different number of slots for the different data types. This means that the data is arriving at disparate rates over the point-to-point links.

- Referring to claim 9, Van As discloses the synchronous switch of Claim 1, wherein the traffic cell comprises asynchronous data, which can be an ATM cell (col. 9, lns. 14-40, col. 10, lns. 9-14).

- Referring to claim 10, Van As discloses the synchronous switch of Claim 1, further comprising: a multiplexer (switch interface) further operable to transmit on the bus an egress frame comprising a plurality of egress time slots that are each operable to transport a slot (traffic cell, col. 23, lns. 1-37); the TX-FSM (switch controller) further operable to determine a queue (an address) in the plurality of queues (switch memory) storing a traffic cell for transport in an egress time slot and to provide the cell form the appropriate queue (address to the switch memory, Fig. 27-29, col. 23, lns. 1-50, col. 24, lns. 27-46); and the queue (switch memory) operable to write the traffic cell at the appropriate queue (address) in the plurality of queues (switch memory) to the egress time slot for transmission on the bus (col. 24, lns. 27-46).

- Referring to claim 11, Van As discloses a switch card for a telecommunications node, comprising: a Pipeline Header Decoder (switch interface) operable to terminate a plurality of point-to-point links operating at disparate rates (Fig. 27-29, col. 8, lns. 13-25, buses inherently

terminate many point-to-point links. The different data types are allocated a different number of slots, so the asynchronous and synchronous data is arriving at disparate rates), to receive from each link a frame having a plurality of time slots that are each operable to transport a traffic cell (Fig. 3-6), to extract a header for a traffic cell from the time slot transporting the traffic cell, and to provide the header to a RX-FSM (switch controller, Fig. 27-29, col. 21, lns. 60-col. 22, lns. 15); the RX-FSM (switch controller) operable to determine a type (synchronous or asynchronous based on the slot type information in the header) for the traffic cell based on the header, to determine based on the type an appropriate queue (an address) for storing the traffic cell in a plurality of queues (switch memory, col. 21, lns. 60-col. 22, lns. 30, the RX-FSM triggers the ADU modifier to split the multi-slot and to direct the traffic to the appropriate queue), and to provide the cell to the appropriate queue (address) to the plurality of queues (switch memory); and the plurality of queues (switch memory) operable to receive the traffic cell from the Pipeline Header Decoder (switch interface) and the appropriate queue (address) for storing the traffic cell from the RX-FSM (switch controller), to associate the queue (address) with the traffic cell, and to store the traffic cell at the queue (address, col. 22, lns. 30-55).

- Referring to claim 12, Van As discloses the switch card of Claim 11, wherein the switch interface, switch controller, and switch memory each operate at a framing period (synchronized frame pulse, col. 24, lns. 60-65).

- Referring to claim 13, Van As discloses the switch card of Claim 12, wherein the frame period (pulse) comprises a 125 microsecond frame period (pulse, Fig. 3-5, col. 12, lns. 1-30).

- Referring to claim 14, Van As discloses the switch card of Claim 11, further comprising: the multiplexer (switch interface) further operable to transmit on each of the

point-to-point links an egress frame comprising a plurality of egress time slots that are each operable to transport a traffic cell (col. 8, lns. 13-25, col. 23, lns. 1-50); the TX-FSM (switch controller) further operable to determine a queue (an address) in the plurality of queues (switch memory) storing a traffic cell to be transported in an egress time slot on a point-to-point link and to allocate the slot to the queue (provide the address to the switch memory); and the plurality of queues (switch memory) operable to write the traffic cell at the appropriate queue (address) in the plurality of queues (switch memory) to the egress time slot for transmission on the point-to-point link (col. 23, lns. 1-50).

- Referring to claim 15, Van As discloses a method for switching traffic at a telecommunications node, comprising: receiving a frame comprising a plurality of time slots each having a traffic cell and a header for the traffic cell (Fig. 3-6, col. 21, lns. 60-col. 22, lns. 15); determining a type for each traffic cell based on the header with slot type information for the traffic cell; determining a queues (address) in the plurality of queues (switch memory) for storing the traffic cell based on the type (synchronous or asynchronous); and storing the traffic cell in the plurality of queues (switch memory) at the appropriate queue (address, Fig. 27-29, col. 21, lns. 60-col. 22, lns. 54).

- Referring to claim 16, Van As discloses the method of Claim 15, further comprising: receiving the frame at a Pipeline Header Decoder (switch interface); extracting the header from the time slots at the Pipeline Header Decoder (switch interface); passing the headers to a RX-FSM (switch controller); and determining to split the multi-slot and to send the data to a queue (address) at the RX-FSM (switch controller) based on the header (col. 21, lns. 60-col. 22, lns. 55).

- Referring to claim 17, Van As discloses the method of Claim 16, further comprising: passing the traffic cell from the Pipeline Header Decoder (switch interface) to the plurality of queues (switch memory); passing the control message to split the multi-slot frame into basic slots to be stored in the appropriate queue (address) from the RX-FSM (switch controller) to the plurality of queues (switch memory); and associating the queue (address) with the traffic cell at the plurality of queues (switch memory, col. 21, lns. 60-col. 22, lns. 55).

- Referring to claim 18, Van As discloses the method of Claim 17, further comprising operating the pipeline header decoder (switch interface), RX-FSM (switch controller), and a plurality of queues (switch memory) at a framing period (synchronized frame pulse, Fig. 3-6, col. 12, lns. 1-30, col. 19, lns. 40-45, col. 24, lns. 60-65).

- Referring to claim 21, Van As discloses the method of Claim 15, further comprising receiving a frame from each of a plurality of point-to-point links of a bus, each frame comprising a plurality of the time slots (Fig. 3-6, col. 8, lns. 13-25). Buses inherently terminate a plurality of point-to-point links. A bus is an electrical connection that allows two or more wires or lines to be connected together.

- Referring to claim 22, Van As discloses the method of Claim 15, further comprising: transmitting an egress frame comprising a plurality of egress time slots that are each operable to transport a traffic cell; determining a queue (address) in the plurality of queues (switch memory) storing a traffic cell for transport in an egress time slot; and writing the traffic cell from the queue (at the address) in the plurality of queues (switch memory) to the egress time slot for transmission in the egress frame (col. 23, lns. 1-50, col. 24, lns. 27-47).

- Referring to claim 23, Van As discloses the method of Claim 16, further comprising: the multiplexer (switch interface) transmitting an egress frame comprising a plurality of egress time slots that are each operable to transport a traffic cell; the TX-FSM (switch controller) determining a queue (address) in the plurality of queues (switch memory) storing a traffic cell for transport in an egress time slot and providing the cell from the queue (address) to the plurality of queues (switch memory); and the plurality of queues (switch memory) writing the traffic cell at the queue (address) in the plurality of queues (switch memory) to the egress time slot for transmission in the egress frame (col. 23, lns. 1-50, col. 24, lns. 27-47).

- Referring to claim 33, Van As discloses a system for switching traffic at a telecommunications node, comprising: a Pipeline Header Decoder (interface means) for receiving a frame, the frame comprising of a plurality of time slots each having a traffic cell and a header for the traffic cell (Fig. 3-6, and 27-29, col. 21, lns. 60-68); and a RX-FSM (controlling means) for determining a type for each traffic cell of the frame based on the slot type information in the header for the traffic cell (col. 21, lns. 60-col. 22, lns. 15), for determining an appropriate queue (address) in a plurality of queues (data storage means) for storing the traffic cell based on the type, and for initiating a storage of the traffic cell in the data storage means at the determined queue (address, col. 22, lns. 1-55).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 3, 4, 19, 20, and 24-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van As. Referring to claim 3, Van As discloses the synchronous switch of Claim 1, further comprising: the queues (switch memory) comprising a plurality of synchronous (time division multiplex, TDM) memory slots in the synchronous queue and a plurality of asynchronous (asynchronous transfer mode, ATM) memory slots in the asynchronous queue associated with output ports to an output multiplexer (Fig. 27-29, col. 22, lns. 30-68); and the RX-FSM (switch controller) further operable to determine an asynchronous queue (an address of an ATM queue) in the plurality of queues (switch memory) for storing a traffic cell in response to determining the traffic cell is asynchronous (of an ATM type, col. 2, lns. 30-40, col. 22, lns. 1-40) and to determine an address of a synchronous (TDM memory slot) in the switch memory for storing a traffic cell in response to determining the traffic cell is synchronous (of a TDM type, col. 22, lns. 1-40). Van As does not expressly disclose that the synchronous data is of the TDM type. The system of Van As could be modified so that the synchronous data is of the TDM type. At the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify the system of Van As to have the synchronous data be of the TDM type. One of ordinary skill in the art would have been motivated to do this since the TDM format is a well-known and widely used synchronous data format for transmitting time-sensitive data, such as voice and video (col. 3, lns. 5-15). Synchronous data and TDM data both need a clock signal to preserve their order.

- Referring to claim 4, Van As discloses the synchronous switch of Claim 3, further comprising: the Pipeline Header Decoder (switch interface) operable to extract a header for the

traffic cell from a time slot transporting the traffic cell and to provide the header to the RX-FSM (switch controller, col. 21, lns. 60-col. 22, lns. 30); and the RX-FSM (switch controller) further operable to determine whether the traffic cell is synchronous or asynchronous (of the ATM type or the TDM type) based on the slot type information in the header (col. 22, lns. 1-40).

- Referring to claim 19, Van As discloses the method of Claim 15, wherein the plurality of queues (switch memory) comprises a plurality of synchronous (time division multiplex, TDM) queue (memory) slots in a synchronous queue (the slots for the synchronous data in the queue are from slots that are time division multiplexed together to form a frame) and a plurality of asynchronous transfer mode (ATM) queue slots associated with output ports (Fig. 27-29, col. 22, lns. 30-55), further comprising determining a queue (address) for asynchronous data (of an ATM queue) in the plurality of queues (switch memory) for storing a traffic cell in response to determining the traffic cell is asynchronous, which can be of an ATM type (col. 9, lns. 20-30, col. 10, lns. 9-13, col. 21, lns. 60-col. 22, lns. 5, col. 22, lns. 35-55). Synchronous data and TDM data both require a clock to preserve their order.

- Referring to claim 20, Van As discloses the method of Claim 19, further comprising determining a queue (address) of a synchronous (TDM) memory slot in the plurality of queues (switch memory) for storing a traffic cell in response to determining the traffic cell is of a synchronous (TDM) type (col. 22, lns. 30-55). Van As does not expressly disclose that the synchronous data is of the TDM type. The system of Van As could be modified so that the synchronous data is of the TDM type. At the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify the system of Van As to have the synchronous data be of the TDM type. One of ordinary skill in the art would have been

motivated to do this since the TDM format is a well-known and widely used synchronous data format for transmitting time-sensitive data, such as voice and video (col. 3, lns. 5-15). Synchronous data and TDM data both need a clock signal to preserve their order.

- Referring to claim 24, Van As discloses the system for switching traffic at a telecommunications node, comprising: (a computer-readable medium; and software stored on the computer-readable medium, the software) operable to receive a frame comprising of a plurality of time slots each having a traffic cell and a header for the traffic cell (Fig. 3-6), to determine a type for each traffic cell based on the header for the traffic cell (col. 21, lns. 60-col. 22 lns. 10), to determine an appropriate queue (address) in a plurality of queues (switch memory) for storing the traffic cell based on the type (synchronous or asynchronous), and to store the traffic cell in the appropriate queue (switch memory at the address, Fig. 27-29, col. 22, lns. 1-55). Van As does not expressly disclose having a computer-readable medium with software stored on the computer readable medium to perform this task. The system of Van As is hardware system. The system of Van As could be modified to be purely software base. At the time the invention was made, it would have been obvious to one of ordinary skill in the art to make the system of Van As in software to process the frames. One of ordinary skill in the art would have been motivated to do this since software gives a designer more flexibility to modify the system. Hardware is hardwired and cannot be easily modified without have to reconstruct the device. One the other hand software only requires modifying the code and recompiling the code in order to accommodate any design changes. This makes software more flexible than hardware. Most devices that can be made in hardware can be programmed into software. Since this device is for frame processing, it could be made entirely in software.

- Referring to claim 25, Van As discloses the system of Claim 24 the software comprising a pipeline header decoder (switch interface) and a RX-FSM (switch controller), the software further operable to receive the frame at the pipeline header decoder (switch interface), to extract the header from the time slots at the pipeline header decoder (switch interface, col. 21, lns. 60-col. 22, lns. 20), to pass the header to the RX-FSM (switch controller), and to determine the that the multi-slot data needs to be parsed and sent to different queues (address) at the RX-FSM (switch controller) based on the header (Fig. 27-29, col. 21, lns. 60-col. 22, lns. 55).

- Referring to claim 26, Van As discloses the system of Claim 25, the software further operable to pass a traffic cell from the pipeline header decoder (switch interface) to the plurality of queues (switch memory), to pass the control signal from the RX-FSM instructing the ADU modifier to split the multi-slot data to be placed into appropriate queues (address) from the RX-FSM (switch controller) to the plurality of queues (switch memory), and to associate the queue (address) with the traffic cell at the plurality of queues (switch memory, col. 22, lns. 15-55).

- Referring to claim 27, Van As discloses the system of Claim 26, the software further operable to operate the Pipeline Header Decoder (switch interface), RX-FSM (switch controller), and a plurality of queues (switch memory) at a framing period (synchronized frame pulse, Fig. 3-6, 27-29, col. 12, lns. 1-30, col. 19, lns. 40-45,col. 24, lns. 60-65).

- Referring to claim 28, Van As discloses the system of Claim 24, wherein the switch memory comprises a plurality of synchronous (time division multiplex, TDM) queue (memory) slots in the synchronous queue and a plurality of asynchronous transfer mode (ATM) slots in the asynchronous queue associated with output ports, the software-further operable to determine (an address of) an asynchronous (ATM) queue in the plurality of queues (switch memory) for storing

a traffic cell in response to determining the traffic cell is of an asynchronous type, which can be an ATM type (Fig. 3-6, col. 22, lns. 1-55). Van As does not expressly disclose that the synchronous queues have TDM memory slots. The system of Van As could be modified so that the synchronous queue is TDM memory slots. At the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify the system of Van As to have the synchronous data be of the TDM type. One of ordinary skill in the art would have been motivated to do this since the TDM format is a well-known and widely used synchronous data format for transmitting time-sensitive data, such as voice and video (col. 3, lns. 5-15). Synchronous data and TDM data both need a clock signal to preserve their order.

- Referring to claim 29, Van As discloses the system of Claim 28, the software further operable to determine an address of a TDM memory slot in the synchronous queue (switch memory) for storing a traffic cell in response to determining the traffic cell is of a synchronous (TDM) type. Van As does not expressly disclose that the synchronous data is of the TDM type. The system of Van As could be modified so that the synchronous data is of the TDM type. At the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify the system of Van As to have the synchronous data be of the TDM type. One of ordinary skill in the art would have been motivated to do this since the TDM format is a well-known and widely used synchronous data format for transmitting time-sensitive data, such as voice and video (col. 3, lns. 5-15).

- Referring to claim 30, Van As discloses the system of Claim 24, the software further operable to receive a frame from each of a plurality of point-to-point links of a bus, each frame comprising a plurality of time slots (Fig. 3-6, col. 8, lns. 13-25). A bus is an electrical

connection that allows two or more wires or lines to be connected together. Thus the system is able to receive a frame from any of these connections over the bus.

- Referring to claim 31, Van As discloses the system of Claim 24, the software further operable to transmit an egress frame comprising a plurality of egress time slots that are each operable to transport a traffic cell, to determine a queue (address) in the plurality of queues (switch memory) storing a traffic cell for transport in an egress time slot, and to write the traffic cell at the queue (address) in the plurality of queues (switch memory) to the egress time slot for transmission in the egress frame (col. 22, lns. 55-col. 23, lns. 50).

- Referring to claim 32, Van As discloses the system of Claim 25, the software comprising: the multiplexer (switch interface) operable to transmit an egress frame comprising a plurality of egress time slots that are each operable to transport a traffic cell; the TX-FSM (switch controller) operable to determine an appropriate queue (address) in the plurality of queues (switch memory) storing a traffic cell for transport in an egress time slot and to provide the cell from the queues (address to the switch memory); and the plurality of queues (switch memory) operable to write the traffic cell at the appropriate queue (address) in the plurality of queues (switch memory) to the egress time slot for transmission in the egress frame (Fig. 27-29, col. 22, lns. 55-col. 23, lns. 50).

Response to Arguments

7. Applicant's arguments, see pages 8-12, filed 06/26/03, with respect to the rejection(s)of claim(s) 1-33 under 103(a) have been fully considered and are persuasive. Therefore, the

rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Van As et al (USP 5,327,428).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher M Swickhamer whose telephone number is (703) 306.4820. The examiner can normally be reached on 8:00-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on (703) 305.4798. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305.3900.

CMS

RICKY NGO
PRIMARY EXAMINER